

TrenchMOS™ transistor Logic level FET

BUK9606-55A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology the device features very low on-state resistance. It is intended for use in automotive and general purpose switching applications.

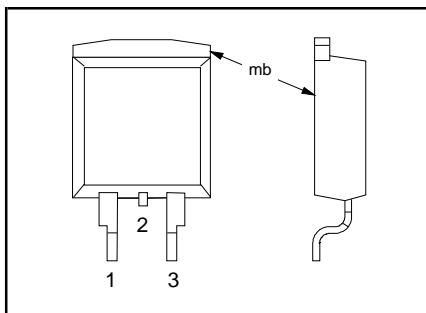
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	230	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	6.3	mΩ
	$V_{GS} = 5\text{ V}$	5.8	mΩ
	$V_{GS} = 10\text{ V}$		

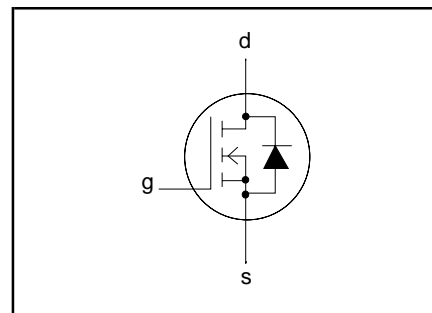
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain (no connection possible)
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50\mu\text{s}$	-	15	V
I_D	Drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	75	A
I_D	Drain current (DC)	$T_{mb} = 100\text{ }^\circ\text{C}$	-	75	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	240	A
P_{tot}	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	230	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	0.65	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

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STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA; T _j = -55 °C	55 50	- -	- -	V V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA T _j = 175 °C T _j = -55 °C	1 0.5 -	1.5 - -	2.0 - 2.3	V V V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 55 V; V _{GS} = 0 V; T _j = 175 °C	- -	0.05 -	10 500	μA μA
I _{GSS}	Gate source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	-	2	100	nA
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A T _j = 175 °C V _{GS} = 10 V; I _D = 25 A V _{GS} = 4.5 V; I _D = 25 A	- - -	5.3 - 4.8	6.3 13.2 5.8	mΩ mΩ mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C _{iss}	Input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	6500	8600	pF
C _{oss}	Output capacitance		-	1000	1200	pF
C _{rss}	Feedback capacitance		-	650	850	pF
t _{d on}	Turn-on delay time	V _{DD} = 30 V; R _{load} = 1.2 Ω;	-	45	65	ns
t _r	Turn-on rise time	V _{GS} = 5 V; R _G = 10 Ω	-	180	270	ns
t _{d off}	Turn-off delay time		-	420	590	ns
t _f	Turn-off fall time		-	235	330	ns
L _d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L _s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

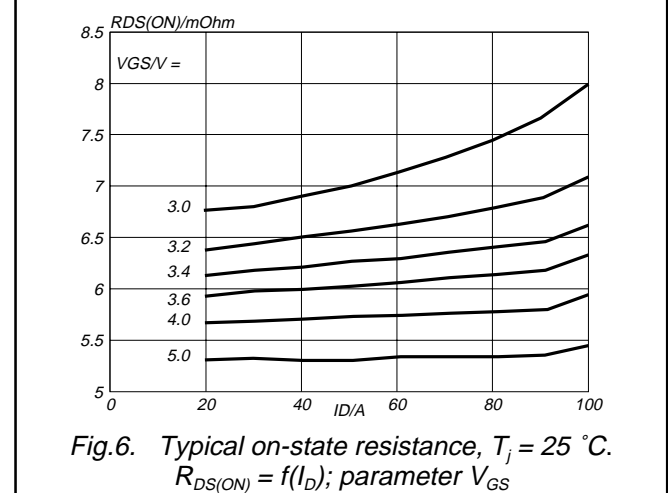
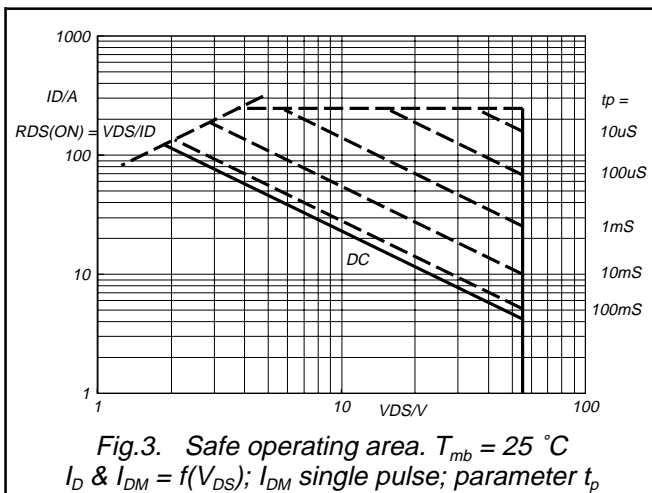
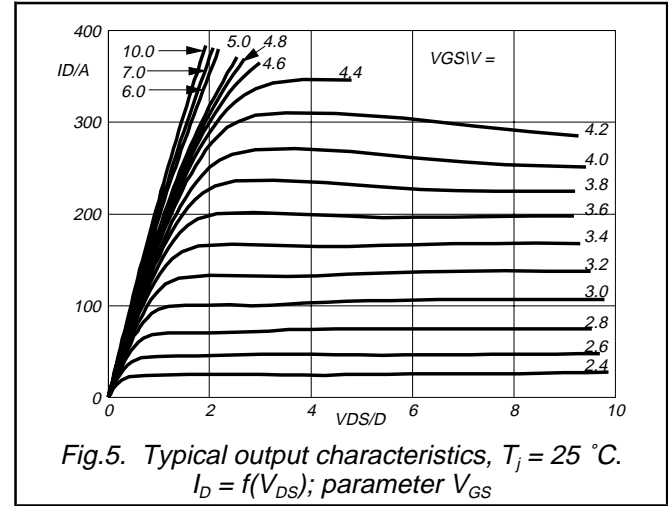
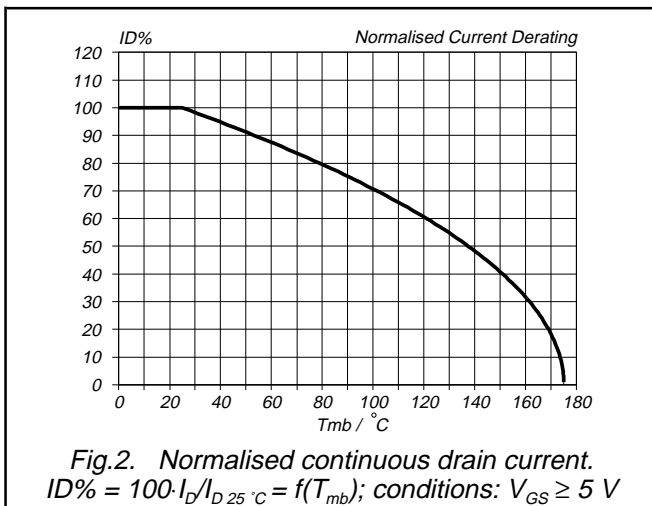
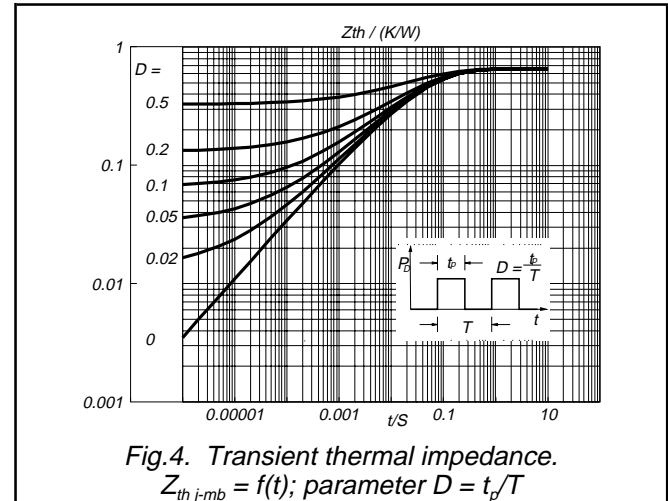
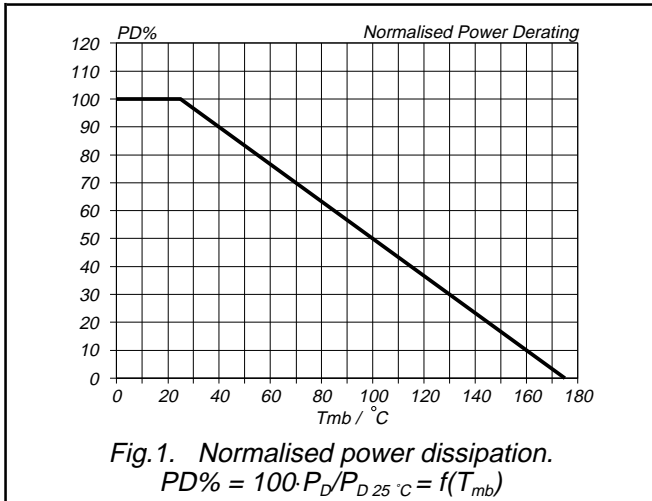
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{DR}	Continuous reverse drain current		-	-	75	A
I _{DRM}	Pulsed reverse drain current		-	-	240	A
V _{SD}	Diode forward voltage	I _F = 25 A; V _{GS} = 0 V I _F = 75 A; V _{GS} = 0 V	- -	0.85 1.1	1.2 -	V V
t _{rr}	Reverse recovery time	I _F = 75 A; -di _F /dt = 100 A/μs;	-	80	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = -10 V; V _R = 30 V	-	0.2	-	μC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W _{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I _D = 75 A; V _{DD} ≤ 25 V; V _{GS} = 5 V; R _{GS} = 50 Ω; T _{mb} = 25 °C	-	-	500	mJ

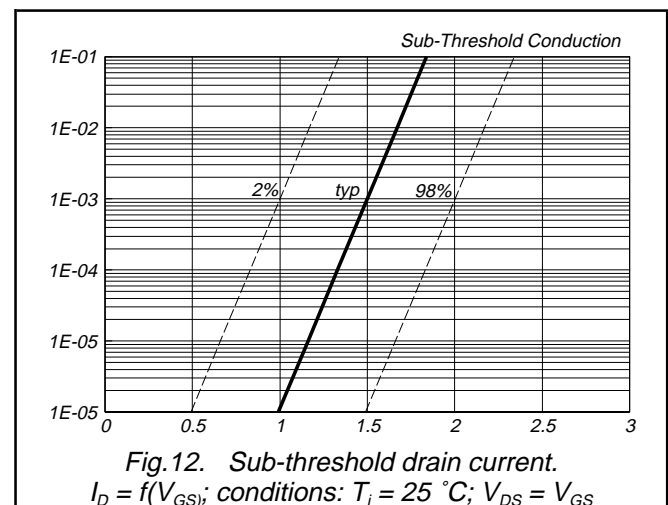
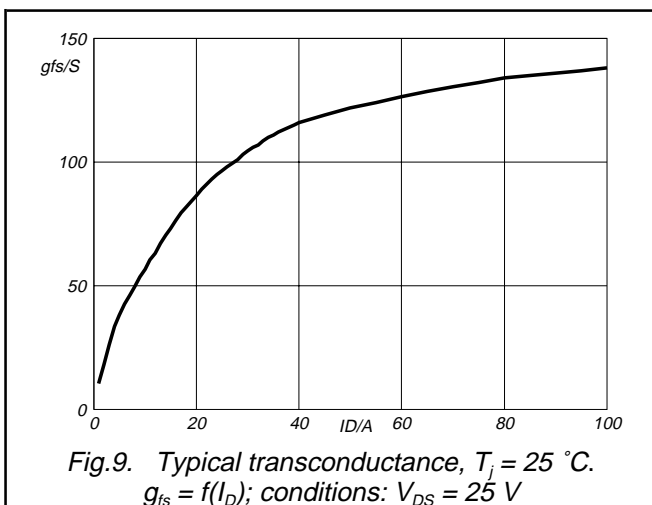
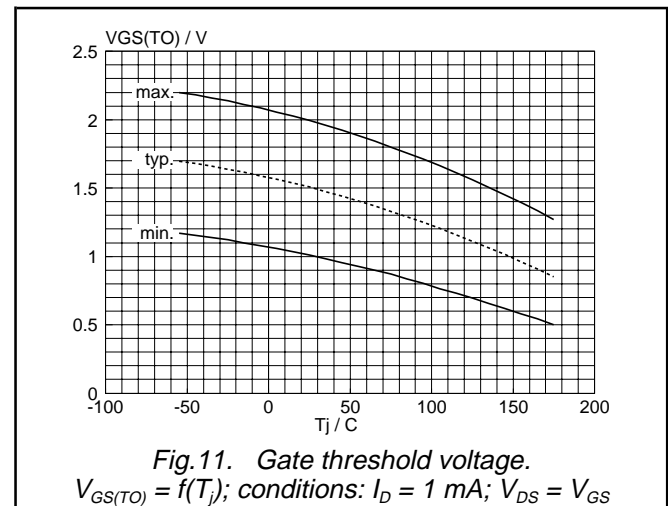
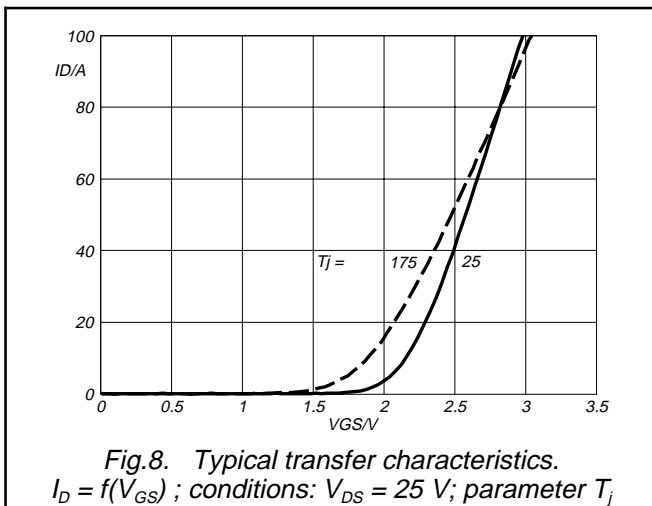
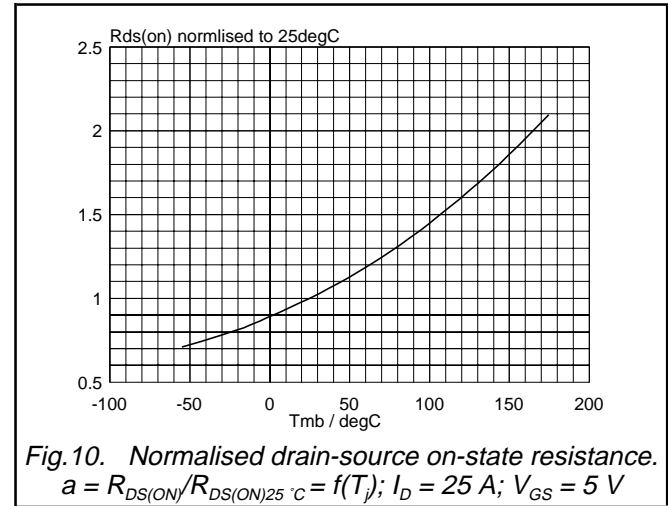
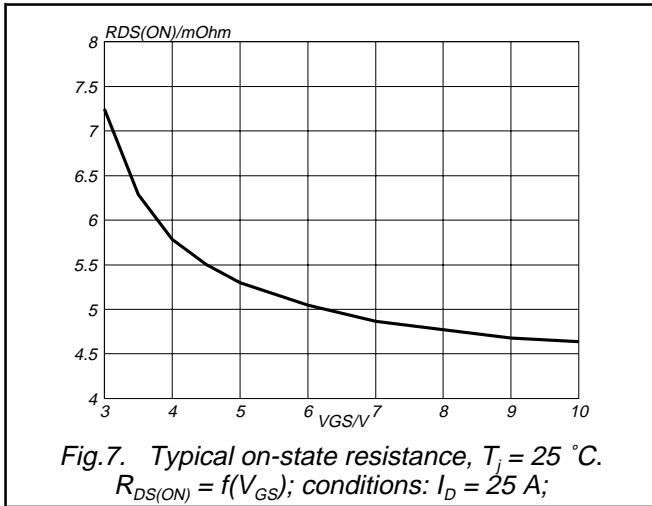
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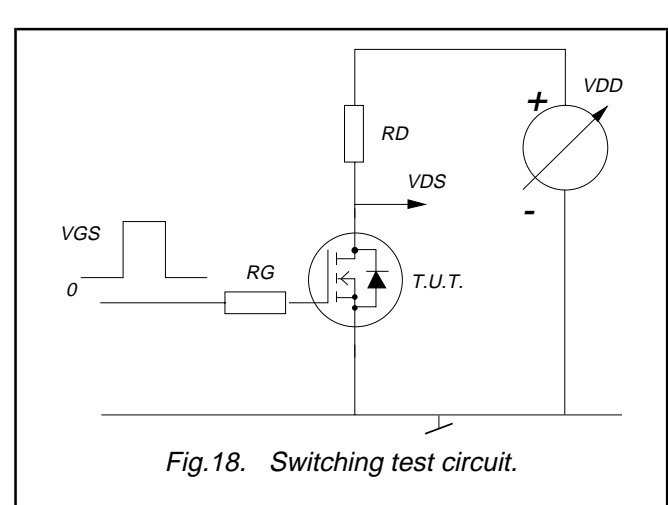
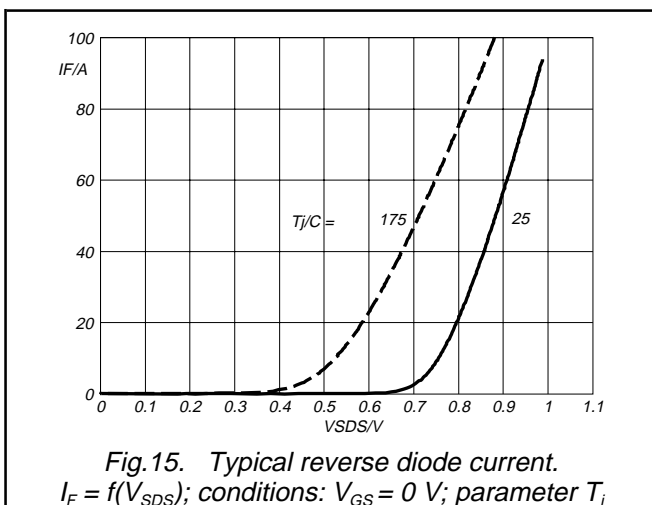
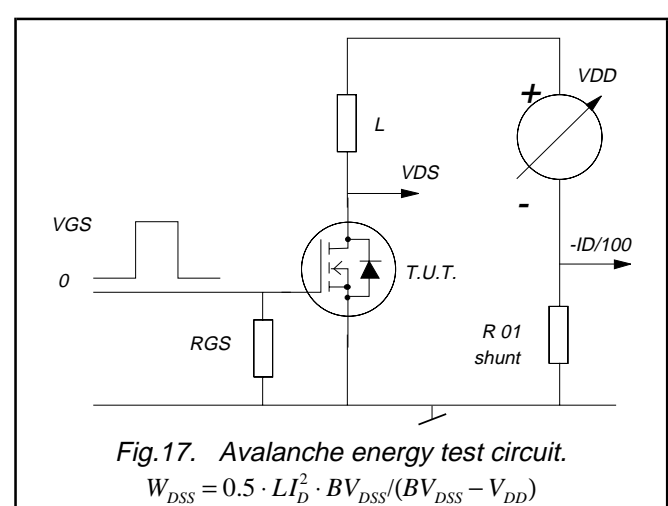
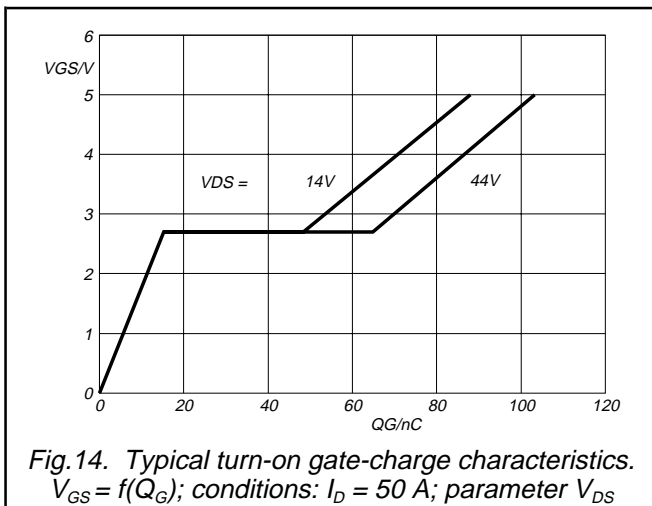
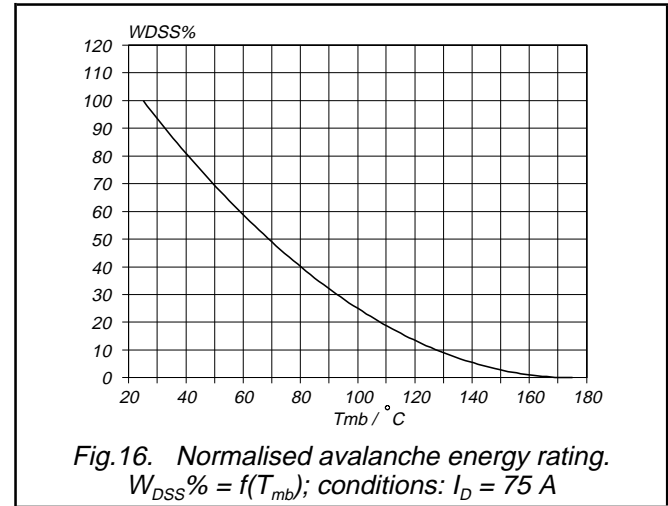
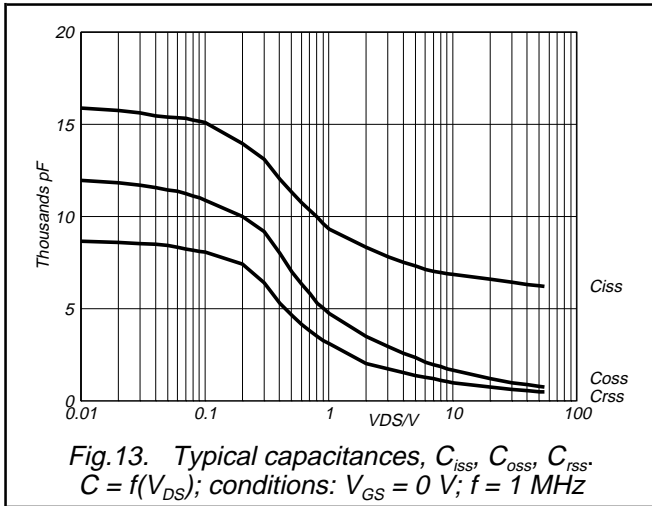
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MECHANICAL DATA

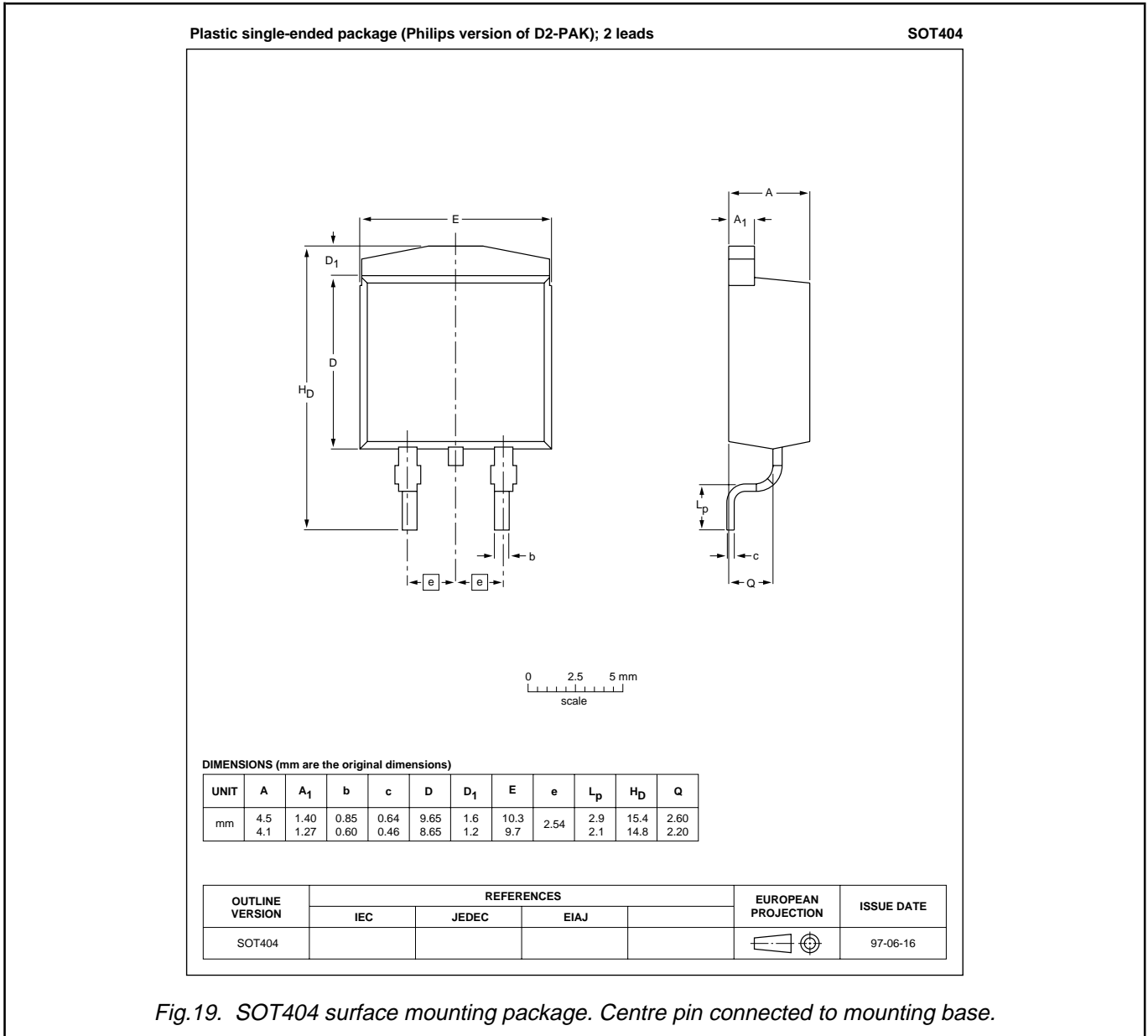


Fig.19. SOT404 surface mounting package. Centre pin connected to mounting base.

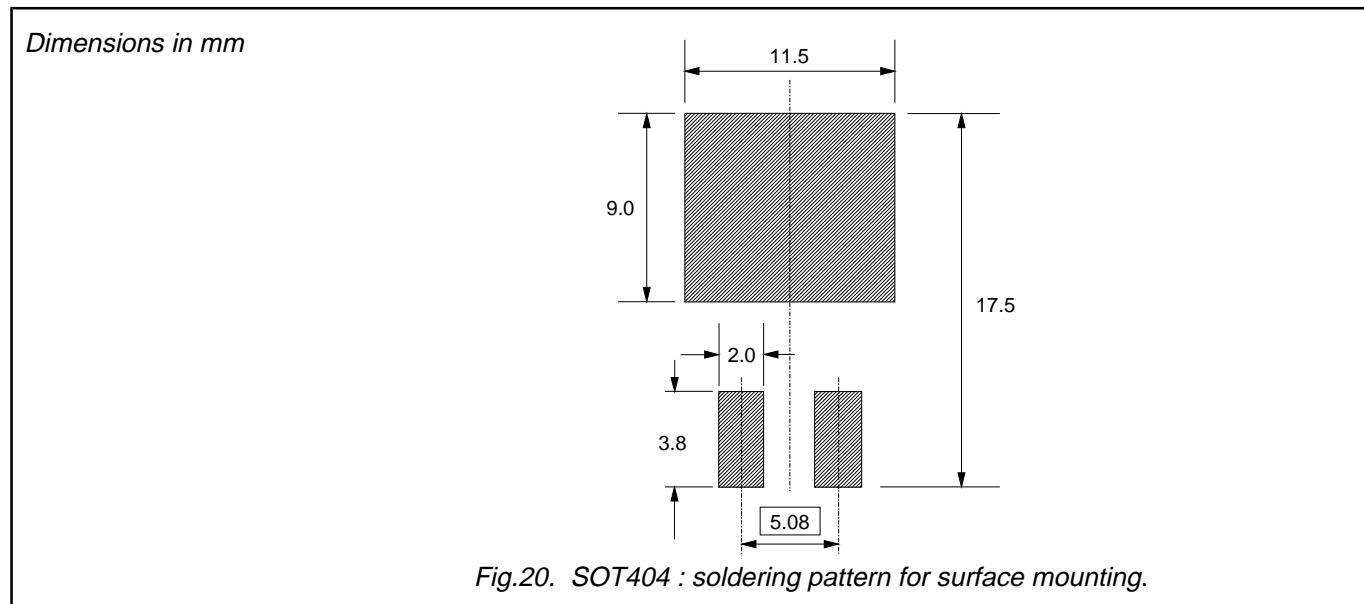
Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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MOUNTING INSTRUCTIONS



DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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